

FQH70N10

100V N-Channel MOSFET

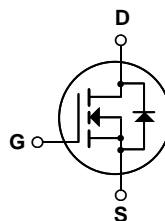
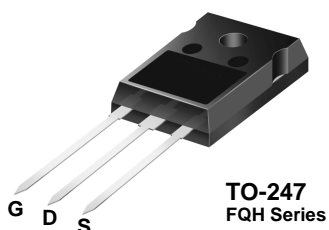
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as audio amplifier, high efficiency switching DC/DC converters, and DC motor control.

Features

- 70A, 100V, $R_{DS(on)} = 0.023\Omega @ V_{GS} = 10V$
- Low gate charge (typical 85 nC)
- Low Crss (typical 150 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- 175°C maximum junction temperature rating



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	FQH70N10	Units
V _{DSS}	Drain-Source Voltage	100	V
I _D	Drain Current - Continuous (T _C = 25°C) - Continuous (T _C = 100°C)	70	A
		49.5	A
I _{DM}	Drain Current - Pulsed (Note 1)	280	A
V _{GSS}	Gate-Source Voltage	± 25	V
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	1300	mJ
I _{AR}	Avalanche Current (Note 1)	70	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	21.4	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	6.0	V/ns
P _D	Power Dissipation (T _C = 25°C) - Derate above 25°C	214	W
		1.43	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +175	°C
T _L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
R _{θJC}	Thermal Resistance, Junction-to-Case	--	0.7	°C/W
R _{θCS}	Thermal Resistance, Case-to-Sink	0.24	--	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient	--	40	°C/W

Electrical CharacteristicsT_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	100	--	--	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	--	0.1	--	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 100 V, V _{GS} = 0 V	--	--	1	μA
		V _{DS} = 80 V, T _C = 150°C	--	--	10	μA
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 25 V, V _{DS} = 0 V	--	--	100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -25 V, V _{DS} = 0 V	--	--	-100	nA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.0	--	4.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 35 A	--	0.019	0.023	Ω
g _{FS}	Forward Transconductance	V _{DS} = 40 V, I _D = 35 A (Note 4)	--	48	--	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz	--	2500	3300	pF
C _{oss}	Output Capacitance		--	720	940	pF
C _{rss}	Reverse Transfer Capacitance		--	150	200	pF

Switching Characteristics

t _{d(on)}	Turn-On Delay Time	V _{DD} = 50 V, I _D = 70 A, R _G = 25 Ω (Note 4, 5)	--	30	70	ns
t _r	Turn-On Rise Time		--	470	950	ns
t _{d(off)}	Turn-Off Delay Time		--	130	270	ns
t _f	Turn-Off Fall Time		--	160	330	ns
Q _g	Total Gate Charge	V _{DS} = 80 V, I _D = 70 A, V _{GS} = 10 V (Note 4, 5)	--	85	110	nC
Q _{gs}	Gate-Source Charge		--	16	--	nC
Q _{gd}	Gate-Drain Charge		--	42	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current	--	--	70	A	
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	280	A	
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 70 A	--	--	1.5	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 70 A,	--	110	--	ns
Q _{rr}	Reverse Recovery Charge	dI _F / dt = 100 A/μs (Note 4)	--	430	--	nC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 0.4mH, I_{AS} = 70A, V_{DD} = 25V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 70A, di/dt ≤ 300A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Characteristics

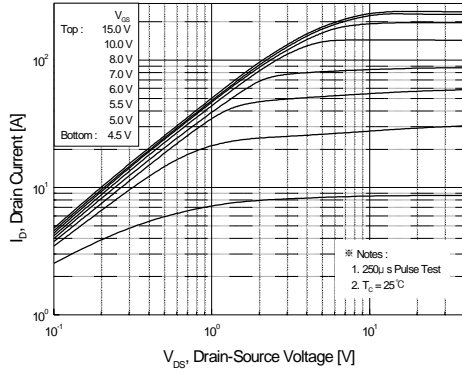


Figure 1. On-Region Characteristics

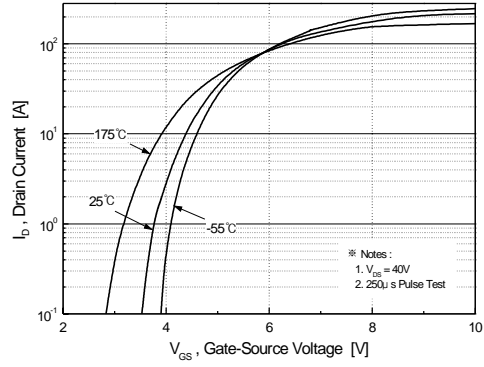


Figure 2. Transfer Characteristics

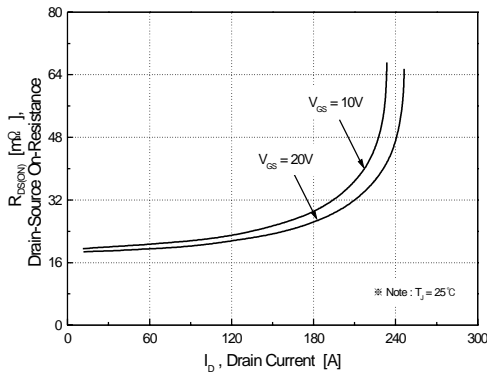


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

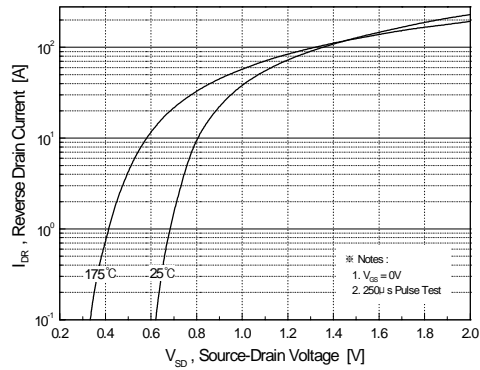


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

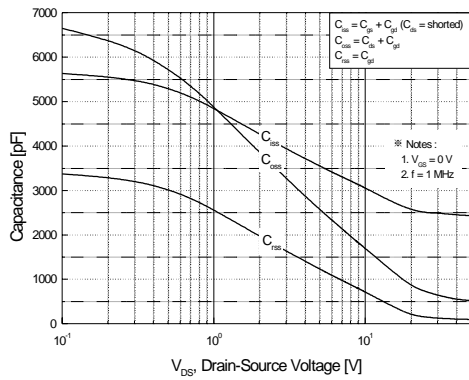


Figure 5. Capacitance Characteristics

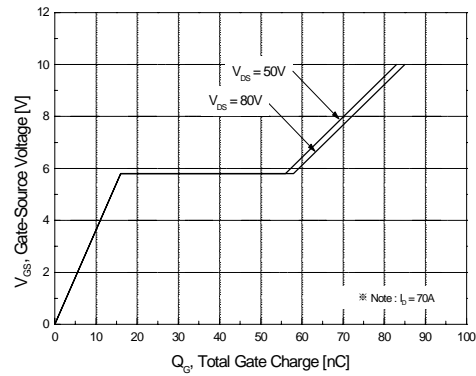


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

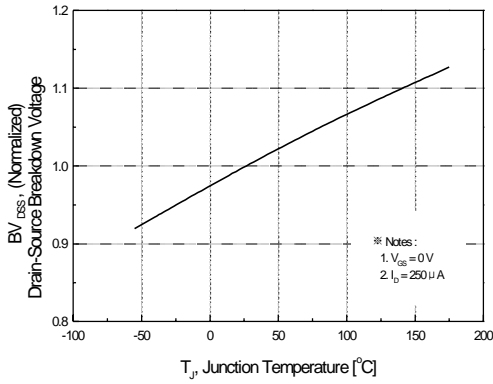


Figure 7. Breakdown Voltage Variation vs. Temperature

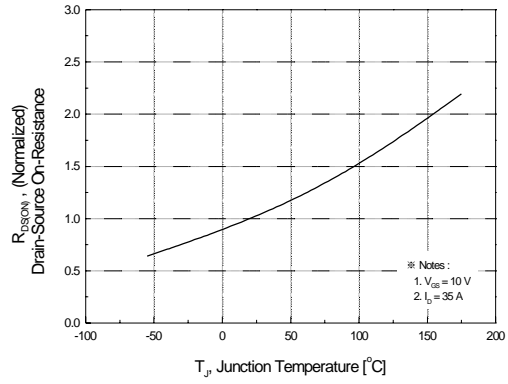


Figure 8. On-Resistance Variation vs. Temperature

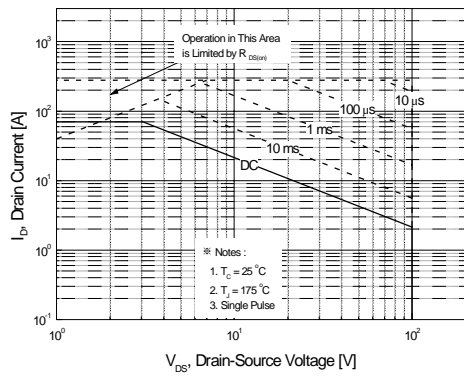


Figure 9. Maximum Safe Operating Area

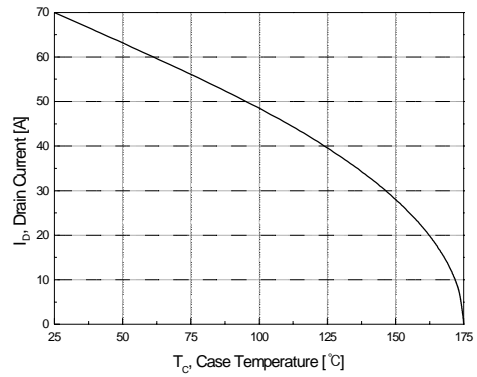


Figure 10. Maximum Drain Current vs. Case Temperature

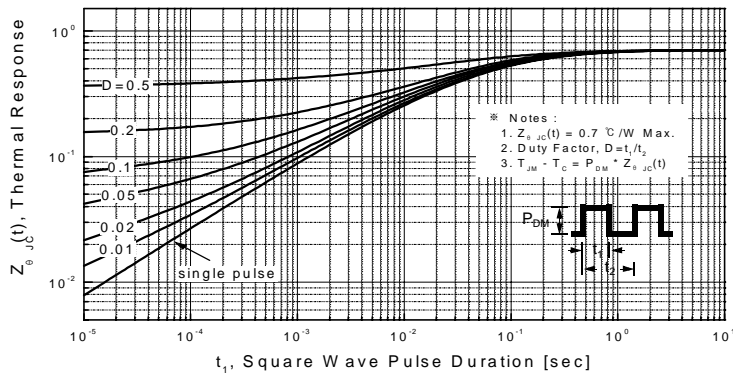


Figure 11. Transient Thermal Response Curve

Gate Charge Test Circuit & Waveform



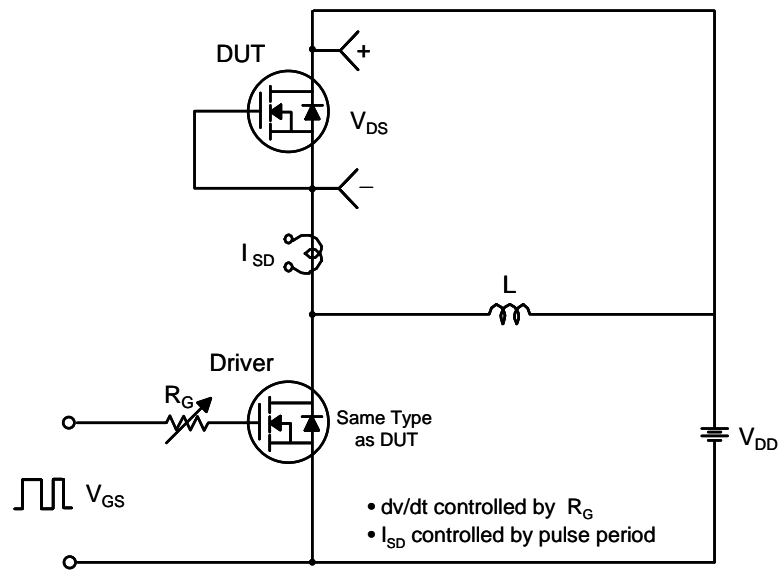
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



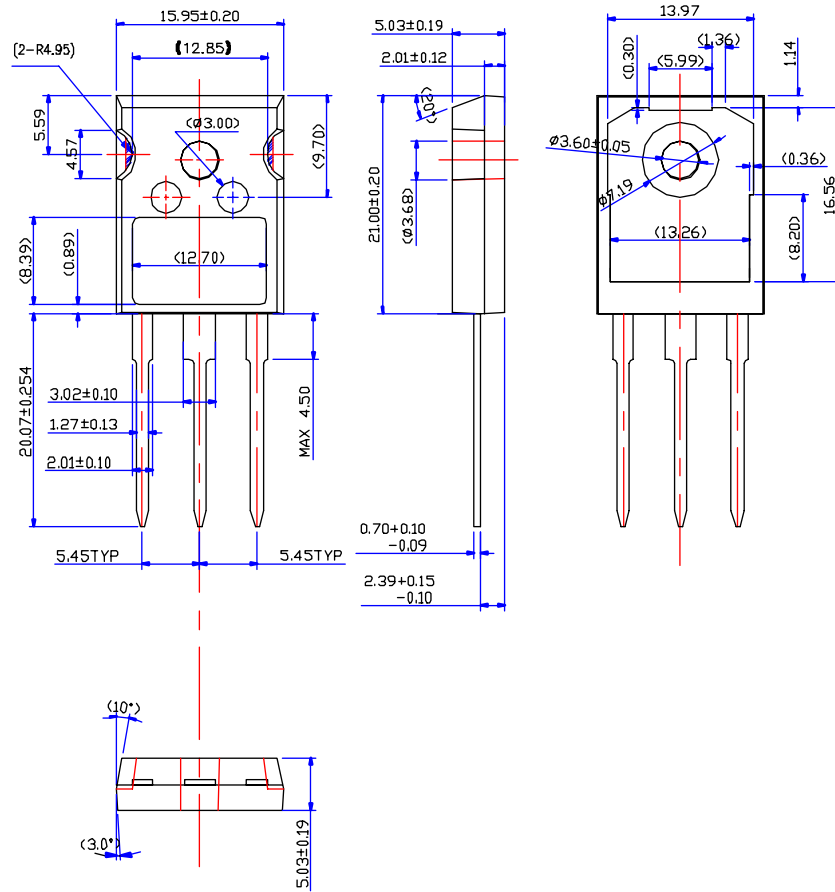
Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimensions

TO-247AD (FKS PKG CODE 001)

FQH70N10



Dimensions in Millimeters

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